POWER ELECTRONICSUK
Underpinning Research

EPSRC
Pioneering research and skills

Newsletter – Summer 2015

Funding Opportunities

The centre continues to support the Research Funding Exchange Scheme. Funding is available for researchers who wish to take an overseas secondment to initiate a collaborative project with external research organisation and for external researchers who wish to initiate a collaborative project with a UK University, affiliated to the EPSRC Centre for Power Electronics.
www.powerelectronics.ac.uk/power-electronics/funding-calls/funding-opportunities

Doctorate Scheme

The new Centre for Power Electronics Doctorate Scheme aims to address the skills shortage by providing doctoral training through a close partnership between Universities and industry. This is a unique opportunity to undertake a doctorate in Power Electronics, working in partnership with a leading university and industry. The doctorate gives an industrial outlet and perspective on research, which is awarded for 3.5 years and includes fees and substantial bursary. Successful candidates will gain industrial experience and training opportunities alongside world-leading research groups. For further information please see our web page.

www.powerelectronics.ac.uk/power-electronics/skills-and-training

Annual Conference

Our second annual conference was held at the National College, Nottingham from the 29th – 30th June 2015, which was sponsored by ETPS and MDL Technologies. The conference featured presentation showcasing research from across the four CPE themes and the three cross-cutting topic. We also were lucky to have as keynote speakers Dr Dushan Boroyevich from The Bradley Department of Electrical and Computer Engineering at Virginia Tech. In addition to speakers Dr Richard McMahon from University of Cambridge, Leigh Murray from University of Warwick, Carl Baker chief Engineer from Alston Grid UK, Prof Mike Barnes from University of Manchester and Prof Stephen Finney from the University of Strathclyde. The conference was extremely well attended with a good mix of delegates from both industry and academia. Copies of presentations can be downloaded from our webpage.
www.powerelectronics.ac.uk/power-electronics/events/pastevents

Annual PG Summer School

Newcastle University kindly hosted the first annual Postgraduate Summer School on behalf of the Centre for Power Electronics, giving a platform for post graduates working in the field of power electronics to engage with other PG students, academics and members of industry. The event included a keynote address by Prof. Bill Drury, a career

workshop, industry fair, oral and poster presentations, panel discussions including networking lunches and an excellent evening dinner social event, which was enjoyed by all.
www.powerelectronics.ac.uk/power-electronics/events/pastevents

EPSRC Mid-Term Review Panel feedback

The panel commend the EPSRC Power Electronics Centre ("the Centre") for bringing together leading power electronics research capability and developing an extensive and challenging research portfolio in an area that did not have an appropriate UK focus point previously. It is considered that without the formation of the Centre this cohesive power electronics focused group would not have been formed. The Centre through its consequent and unprecedented new collaborations and ventures, including those with researchers outside the more traditional power electronics community, has resulted in a clear identity for power electronics in the UK. A particular highlight was the opportunity to meet the new generation of researchers who have the clear potential to be internationally-leading researchers in power electronics.

Research Highlights

Components theme

Components theme are investigating 3D FE model of an amorphous metal-cored high-current, high-frequency inductor (200 A, 150 kHz) established, focussing particularly gap losses. The 3D FE steady-state thermal simulations of the potted inductor undertaken and used to optimise the; can design, the embedded heat spreader and investigate the feasibility of using ceramic coatings**.** DC-DC converter for testing high-power inductors (60 kW continuous, 90 kW peak) are under construction. Completed tasks include the inductor fabrication, the design, construction and assembly of PCBs for gate drivers and current transducers. The controller is currently under development**.** SiC class E inverter with custom GaN resonant gate drive designed, built and tested. Performance benchmarked against original inverter based in silicon switches using off- the-shelf gate drive: Efficiency savings as expected (94% versus 82% at 100W), Resonant gate drive switches SiC FET reliably in class E, Measured power consumption (<2 W) of custom gate drive 3 times lower than measured off-the-shelf gate drive (~6 W). Design for Reliability and Robustness: Further analysis of 2D and 3D FEA methods have been carried out. Parameters for Clech's algorithm have been obtained using 2D FEA for solder joint thickness from 0.2 to 0.5mm**.** Deliverable D4.3 (Initial report detailing reduced order stress models and physics-of-failure models) has been submitted. Design for electro-thermal management: A 5kW DC-DC Boost converter has been designed and analysed: Temperatures in all components are predicted, Losses are calculated from circuit simulation, Losses are fed into FEA model, FE thermal parameter extracted. Passive components thermal analysis based on FEA method.

Components has also welcomed Dr Joyce Wang (Bristol) to the team, she has started work on active gate driving.

Converters theme

High Power DC-DC Topologies A two-level dual active bridge DC-DC converter module is being designed and constructed using silicon carbide devices (15 kW, 50 kHz, 1kV). The component selection and busbar design has been completed and the system is being assembled. Test results are anticipated by the end of the summer.

Topologies for Compact Converters Research on the application of super junction MOSFETS (Neville McNeill) is examining their use in impedance ("Z")-source converters. The limited DC link current into the inverter at transistor turn on is expected to assist in controlling the turn on transient. Initial single

phase-leg tests have been promising and a three-phase, 270 V 3.5 kVA inverter is now being prototyped.

PhD student Bosen Jin has prototyped the four-level π-type converter using IGBTs. Initial test results at 10 kHz and 50 kHz confirm the output waveform quality and efficiency predictions (efficiency >97.5 % at 2 kW). In the next quarter the neutral point balancing algorithm will be implemented and evaluated.

Topologies for Compact Converters New RA, Dr Behzad Ahmadi, started in mid-June working on AC-AC converter concepts. The work will focus on integrated passive components for inclusion in the power semiconductor package, the objectives being to minimise the number of system components, and to minimise the potential negative impact of wide band-gap devices, namely increased EMI filtering requirements. A test bed for the determination of integrated inductor performance and characteristics is under development.

Structural and Functional Integration RA Dr Xi Lin has continued the development of a low inductance blade connector concept for power device modules and DC link capacitors. The conceptual design has been finalised and comprises a multiple receiving slot structure and co-axial terminal connection to the film capacitor. Connection inductances of a few nH are predicted, an order of magnitude lower than the figure for screw connections. A demonstration prototype will be developed in the next quarter.

Design Tools and Optimisation RA Dr Ian Laird has continued the development of design optimisation techniques for DC-AC converters including the line filtering required to meet typical aerospace power quality requirements. Mass and weight optimised solutions have been generated. To validate the results of the optimisation process a naturally cooled 5 kW converter is being constructed.

Design Tools and Optimisation RA Dr James Scoltock has continued to research design optimization techniques for interleaved DC-DC converters, in particular focusing on the development of a simplified electro-thermal model for the inductor where all the losses are conducted downwards to a water-cooled heatsink. The future work will continue to extend the number of component models and their fidelity and will use the optimization techniques to explore the key design trade-offs in multi-kW systems.

Devices theme

Silicon super-junction devices (600V/1.2kV SJ Trench IGBTs) Experimental results of the latest trial lot have been received (end of June). A trench layer misalignment has caused the gate/source to be short-circuited for some wafers. An amended trial lot is expected by the end of August. Characterisation of the surviving wafers/devices is in progress. Testing is currently done at wafer level (Von and Vbr, at 25C) . Selected dies will be sent for packaging and testing at the package level will be performed. Simulations are also performed when in order explain some unexpected characteristics and to fine tune simulation models to get a better match between simulations and measurements. We have identified some breakdown issues in this batch. Further layout optimisation given the new experimental results is performed.

TCAD models for Si, SiC and GaN devices Additional simulations were performed for SiC-based JFETs to incorporate improved simulation models. Simulation results are in good agreement with the experimental data sets. In addition, TCAD simulations are performed to investigate the edge termination in high-breakdown (~3 kV) voltage devices. D1.1 report is currently being prepared to incorporate developed models and simulation findings.

Silicon Carbide Devices *Fabrication of 10 kV 4H-SiC PiN diodes:* The work on 10kV PiN diode is in progress as well as fabrication and design of devices with novel JTE.
Fabrication of 4H-SiC MOSFET devices: First stage LMOSFET oxidation experiment has been finished. Different oxidation and post oxidation annealing conditions have been applied and a maximum value of low field mobility which can be achieved is 15~17cm^2/(Vs). The existing wafer for LMOSFET processing has already been used up. New quarter wafer are during implantation process, and new mask sets with various gate length will be used this time to make high current density devices. To develop a smooth side wall trench structure is challenging, however it is the key to develop high quality trench MOSFET. The initial effort mainly focused on photo lithography process, the aim is to make the features as smooth as possible in order to not transferring any unexpected striation from the photoresist to trench sidewall. It is nearly finished with photolithography recipe developing.
New high resolution photoresist ECI3012 has arrived, and after finding the best recipe for this photoresist, ICP etching, post annealing and sacrificial oxide growth will be carried out. Following the assessment of the first set of SiC devices from Warwick, a new device specification was developed for the subsequent EL and further experimental assessments. *Fabrication of 4H-SiC MOSFET devices:* MIS mask layout fabricated. Nearly 50% of MIS [Metal/(Al2O3+SIO2)/SIC] structure fabrication work using the low temperature process is completed. n-MOSFETs mask layout is completed and is ready to be sent to Compugraphics to get printed. Refined the process flow for n-MOSFETs fabrication.

Gallium Nitride Devices Modelling effort for buffer design to enable high voltage devices was progressed. The previous quarter activities have continued. In particular, the TCAD simulation study on the properties of GaN as the active material in power devices has continued with trap-states models been included into simulations in order to assess the effect on current collapse, transfer characteristics, gate capacitance and behaviour under steady state and during transient events. A conference publication has been submitted (L. Ethymiou et al. submitted to CAS 2015).

Compact Circuit Models Commercially available devices have been tested and simulated. Simulation models were adjusted to obtain better match with measured data.

Interface Characterisation Repeated thickness measurements on ultra-thin-SiO2/SIC interface using AFM and Ellipsometry. Electrical characterisation is currently underway to examine the electrical properties of SiO2/SIC interface. Work continuing on 4H-SiC lateral MOSFETs to improve the SiC/SiO2 interface to achieve high MOS channel mobility in power devices. The relationship between “Dit” and channel mobility will be investigated. New high current density LMOSFET will be sent to Bristol.

Interface Formation Repeated experiments for ultra-thin growth of SiO2 on SiC epilayers. Measurements have validated the growth of 0.7-1.2 nm SiO2 on epilayers. More thickness analysis is planned using the XPS technique.

Epitaxial Growth of SiC Material Completed deliverable D2.4 on ‘Develop high quality epitaxial material (thick layers)’ in June 2015. Etching experiments are being performed on test wafers in order to achieve the faster and deeper etching while maintaining the desired geometry and smooth surface morphology inside trenches. ~5um deep trenches with a smooth surface morphology has been realised on SiC test wafers. Mask layout for super-junction trench fabrication on test wafers has been finalised and is ready to be sent Compugraphics to get printed. Etched test wafers will be sent back to Warwick to study growth experiments.

Contact degradation
Deliverable 3.4 on Reliable metal contact formation was completed in December and submitted to the CPE. No further work to report. Newcastle will contribute to it once the first batch of devices is complete (status unchanged).

Bulk Si LIGBTs rated at >700V compatible with CMOS power integrated circuits
Characterisation of fabricated lateral IGBTs and MOSFETs has continued. More trade-off curves were generated for al tested LIGBTs (Von vs. Eoff at Tj=125C). Some new effects have been noticed which would allow further improvement of trade-off and lower overall losses in the application. Specialised LIGBT structures which were designed to test various trade-offs between Von and Eoff have been the focus of testing and simulations. First batch of devices tested or reliability has successfully passed >1500h of HTRB stress with 560V. New batch of LIGBTs was put for HTRB stressing with 640V bias. Devices with the interconnection deign are also put under HTRB stress to check if this feature affects reliability. New automated testing system has been developed. The system uses LabView to integrate several pieces of equipment and automate the testing process. Testing can be done at all temperatures between 25C and 200C with only remote interaction from the user. The throughput of testing has significantly improved with the new automated measurement set-up for pulsed testing of HV devices. Using the new automated system more samples of the same designs can be now tested more efficiently to generate more accurate trade-off curves.
Simulations have been continuously performed in parallel with measurement. They are used to explain some unexpected characteristics and to fine tune simulation models to get a better match between simulations and measurements

Bulk Si LDMOSFETs rated at >1000V for power integrated circuits MOSFETs which can support 1000V have also been put under HTRB stress with 800V bias at Tj=125C. This will check if devices can be rated at 1000V (stress is at 80% of the rated voltage). Variation in Vbr has been seen from wafer to wafer which is the result of changing substrate resistivity. This was seen in simulation s as well. Some test structures designed to check if Vbr of the circular edge area in each finger can be improved have shown very promising results. Some designs show even 200V higher Vbr than standard (golden) devices. Capacitances of the packaged MOSFET finger (in DIL24 packages) have been measured. The measured capacitance values are very low although the include parasitic capacitances of the package and the measurement system.

<u>Drives theme</u>

Work in April and May has concentrated on completing demonstrator specification and simulations for drive and front end are now ready for input filter and machine models**.** Drive design work will begin shortly – controller and some ancillary electronics have already been selected**.** Analysis on device type for drive (module vs discrete), input filter and machine designs for demonstrators is underway**.** Work in May concentrated on issues with integrated windings and choice of power components**.** Work in July has concentrated on completing demonstrator specification**.** Work on quantifying parasitic for distributed devices**.** We are pleased to report that VPPC submitted papers have been accepted**.** Experimental work has been progressing on bonding methods and thermal testing for integrating switching devices onto machine windings**.** Laboratory evaluation of Artesis bearing health monitoring unit for PM drives has been completed**.** Lifetime prognostics via temperature monitoring/observation have been established**.** Design optimisation of Fault tolerant PM drive; Failure mode and fault analysis completed and design optimization completed

Best wishes from the CPE team

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